LISTING OF CLAIMS

Claims 1-8 (Canceled).

Claim 9. (Currently Amended): A method of manufacturing a semiconductor substrate having shallow trench isolation regions and a device region sandwiched by the shallow trench isolation regions, without using doped silicon oxide containing a melting temperature lowering dopant for lowering the melting temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) depositing oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting temperature lowering dopant;

(c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(d) ~~annealing~~ changing ring structure of the oxide films, after said removing, by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

Claim 10. (Previously Presented): The method of claim 9, wherein the CVD method is any of atmospheric pressure CVD method, low pressure CVD method, plasma CVD method, photo CVD method, and liquid phase CVD method.

11. (Previously Presented): The method of claim 9, wherein the annealing is carried out in any one of reductive gas such as H_2 insert gas such as He, Ne, AR, Kr, or Xe, O_2, N_2, HCl, CO, and CO_2, or in a gas mixture consisting of any mixture of two kinds of gas selected from these gases.

Claims 12 and 13 (Canceled).

Claim 14. (Original): The method of claim 9, wherein each of said grooves has an aspect ratio $d/1_{1x}$ of less than 10, which is defined by a dimensional ratio of a depth d to a width 1_{1x} of an opening at a top of each of said grooves.

Claim 15. (Original): The method of claim 9, further including arranging said grooves in a cyclic line and space pattern having a line-and-space ratio $1_{1x}/1_{2x}$, of less than 1.5, and defined as a ratio of minimum space width 1_{1x} corresponding to a width of openings of the grooves measured along an axis extending in an x direction to a minimum line width 1_{2x} corresponding to a width of a region sandwiched by said grooves and also measured along said x direction.

Claims 16-23 (Canceled).

Claim 24. (Original): The method of claim 15, wherein each of said grooves has an opening having the width 1_{1x}, and a height 1_{1y} measured along a y direction so as to provide a second line-and-space ratio $1_{1y}/1_{2y}$ which is larger than 1.5, with 1_{2y} being a space between the grooves and measured along the y direction.

Claim 25. (Currently Amended): A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, without using doped silicon oxide containing a melting temperature lowering dopant for lowering the melting temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) depositing oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting temperature lowering dopant;

(c) ~~annealing~~ changing ring structure of the oxide films by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so the dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(d) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

Claim 26. (Currently Amended): A method of manufacturing a semiconductor substrate having a shallow trench isolation, without using doped silicon oxide containing a melting temperature lowering dopant for lowering the melting temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting temperature lowering dopant; and

(c) ~~annealing said~~ changing ring structure of the oxide films by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that ~~said~~ the oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, and an etching rate by ammonium fluoride solution of ~~said~~ the oxide films is less than 130 nm/min, which is substantially identical to that of a thermal oxide film.

Claim 27. (Currently Amended): A method of manufacturing a semiconductor substrate having a shallow trench isolation, without using doped silicon oxide containing a

melting temperature lowering dopant for lowering the melting temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting temperature lowering dopant; and

(c) ~~annealing~~ changing ring structure of the oxide films by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150°C, but less than or equal to 1350°C so that ~~said~~ the oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, the respective predetermined rates of the ring structures are determined according to rates of integrated Raman intensities corresponding to respective ring structures to a total integrated Raman intensity, and the structures are formed to satisfy either of or both conditions that said higher order ring structures are substantially more than 85 % of an overall structure and said lower order ring structures are substantially less than 15 % of the overall structure.

Claim 28. (Currently Amended): A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, without using doped silicon oxide containing a melting temperature lowering dopant for lowering the melting temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by a CVD method using an electrically inert organic silicon source, which does not contain the melting temperature lowering dopant;

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(e) ~~annealing~~ changing ring structure of the oxide films, after said removing, by annealing the semiconductor substrate so as not to melt the oxide filmsat a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

Claim 29. (Currently Amended): A method of manufacturing a semiconductor substrate having a shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, without using doped silicon oxide containing a melting temperature lowering dopant for lowering the melting temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by a CVD method using an electrically inert organic silicon source, which does not contain the melting temperature lowering dopant;

(d) ~~annealing~~ changing ring structure of the oxide films by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(e) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

Claim 30. (Currently Amended): The method of claim 9, wherein ~~said~~ the oxide films are deposited directly on walls of the grooves.

Claim 31. (Currently Amended): The method of claim 25, wherein ~~said~~ the oxide films are deposited directly on walls of the grooves.

Claim 32. (Currently Amended): The method of claim 26, wherein ~~said~~ the oxide films are buried directly on walls of the grooves.

Claim 33. (Currently Amended): The method of claim 27, wherein ~~said~~ the oxide films are buried directly on walls of the grooves.

Claim 34. (Previously Presented): The method of claim 28, wherein said thin thermal oxidation films are formed by thermally oxidizing inner walls of the grooves.

Claim 35. (Previously Presented): The method of claim 29, wherein said thin thermal oxidation films are formed by thermally oxidizing inner walls of the grooves.

36. (Currently Amended) A method for forming a microelectronic structure, without using doped silicon oxide containing a melting temperature lowering dopant for lowering the melting temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a mask layer on a substrate wherein the mask layer exposes a part of the substrate;

(b) forming a groove in the exposed part of the substrate

(c) depositing a layer of an insulating film using an electrically inert source so as to fill the groove and cover the mask layer, which does not contain the melting temperature lowering dopant;

(d) ~~annealing said~~ changing ring structure of the insulating film by annealing the semiconductor substrate so as not to melt the oxide films at a temperature which is greater than or equal to 1150°C but less than or equal to 1350°C.

Claim 37. (Previously Presented): The method of claim 36, wherein said annealing is performed for a period of time of about 1 hour to about 2 hours.

Claim 38. (Previously Presented): The method of claim 36, wherein said annealing is performed for a period of time of about 1 hour.

Claim 39. (Previously Presented): The method of claim 36, wherein said annealing is performed in an inert atmosphere.

Claim 40. (Previously Presented): The method of claim 36, wherein said annealing is performed in an atmosphere of nitrogen (N_2).

Claim 41. (Currently Amended): The method of claim 36, further comprising:

planarizing ~~said~~ the insulating film so that the substrate is exposed.

Claim 42. (Previously Presented): The method of claim 41, wherein said planarizing comprises using a Chemical Dry Etching (CDE) method.

Claim 43. (Previously Presented): The method of claim 36, wherein said forming the mask layer comprises forming an oxide layer on the substrate.

Claim 44. (Previously Presented): The method of claim 36, wherein said forming the layer of the insulating film comprises forming an oxide layer on inner walls of the groove and depositing an insulating material on the oxide layer to fill the groove.

Claim 45. (Previously Presented): The method of claim 44, wherein said depositing the insulating material comprises forming an oxide by a CVD method using the electrically inert source.

Claim 46. (Currently Amended): The method of claim 36, wherein ~~said~~ the insulating film is deposited directly on walls of the groove.

Claim 47. (Canceled).

Claim 48. (Previously Presented): The method of claim 36, wherein said groove tapers.

Claim 49. (Previously Presented): The method of claim 36, wherein said depositing the layer of the insulating film is configured to deposit the insulating film at a thickness larger than a half of a width of the groove.

Claim 50. (Previously Presented): The method of claim 36, wherein said forming the mask is configured to provide a plurality of grooves at a cross sectional view so as to define a SDG region between a couple of the grooves at the cross sectional view.

Claim 51. (Previously Presented): The method of claim 50, wherein said SDG region has a width of 0.3 μm, measured between the couple of the grooves.

Claim 52. (Previously Presented): The method of claim 50, further comprising:

forming source and drain regions in the SDG region sandwiched by the grooves.

Claim 53. (Previously Presented): The method of claim 50, wherein each of the grooves has an aspect ratio d/l_{1x} of less than 10, which is defined by a dimensional ratio of a depth d to a width 1_{1x} of an opening at a top of each of the grooves.